TEMPERATURE ANALYSIS AND ON-CHIP COMPENSATION FOR AN UHF VCO

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Abstract

This paper treats the study of on-chip temperature compensation of a broad-band UHF VCO. Analysis, design and evaluation of IC oscillators are described. Excellent agreement between simulation and measurement is demonstrated. The frequency deviation drift specification over a 25°C temperature range has been reduced to < 0.5 MHz within the frequency range of 470∼930 MHz.

1 Introduction

Temperature stability is one of the most important properties of RF and microwave integrated circuits. Realization of good temperature stability over a wide frequency range is always a challenge. This criterion in the case of a oscillator is the frequency deviation with ambient temperature. Although it is apparent that the theoretical analysis of temperature dependence is essential in achieving stable design, few results in this area have been reported.

This paper systematically describes the temperature analysis and on-chip compensation of a low-voltage VCO used for the UHF band. The study is based on an existing wide-band balanced oscillator realized in Philips' BiCMOS process Qubic-1. The block diagram of the VCO is shown in Figure 1. This work considers: temperature modeling, theoretical and experimental analysis, temperature compensation, and evaluation.

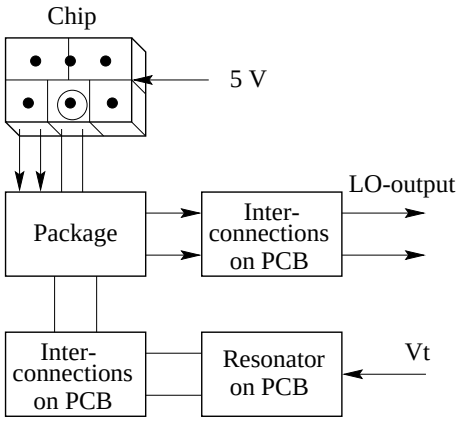

Figure 1: Block diagram of VCO

2 Temperature Modeling

Suitably precise temperature models of IC circuits and components are imperative when carrying out temperature analysis and compensation. It is important to determine the chip temperature T_{chip}, which is the combined effect of ambient temperature and self-heating, since the transistor properties are nonlinearly dependent on this "background" temperature. The steady-state thermal behavior of the chip-package and IC structure can be analyzed approximately using an electrical analog shown in Figure 2 [1] where voltage is analogous to temperature and current

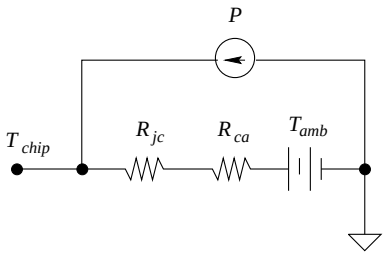

Figure 2: Electrical analog for the thermal behavior of the chip-package structure

related to heat flow represented by the power dissipation

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(P) in the chip, respectively. The resistances R_{jc} and R_{ca} are termed the $junction\text{-}case\ resistance$ and $case\text{-}to\text{-}ambient\ resistance$ of package, respectively. They vary from package to package. Under steady-state conditions the following expression relates the quantities in Figure 2,

$$T_{chip} = T_{amb} + (R_{jc} + R_{ca})P = T_{amb} + T_{ref} \qquad (1)$$

where T_{amb} is the ambient temperature and P the power dissipation on the chip. In practice, the power dissipation of a multi-functional chip is inhomogeneous so that further modeling is required. Figure 3(a) presents the chip in which

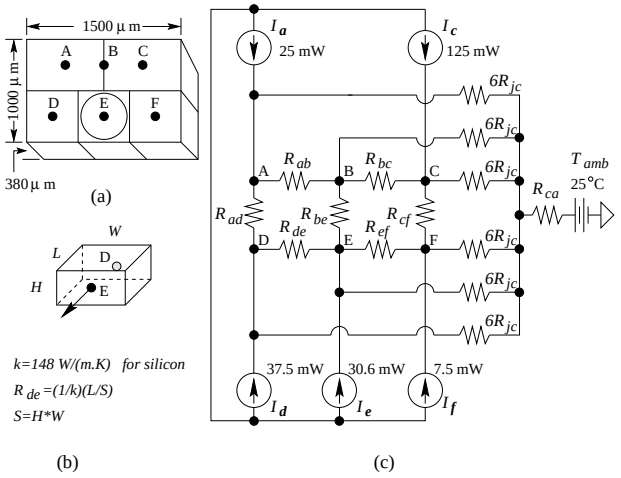

Figure 3: Analog model of heating for chip temperature calculation (a) Chip division, (b) Calculation of thermal resistance between A and B on silicon; (c) Electrical analog model

our oscillator is integrated. Considering various power dissipations for the five different blocks of the chip, a new analog model given in Figure 3(c), as an extension to the model in [1], is created for calculating the temperature of each block. The calculation of thermal resistances between the nodes is given in Figure 3(b). The chip temperature of the VCO located within block E can be easily obtained by calculating the voltage of node E. The temperatures at five nodes, as given in Table 1, are slightly different due to the small thermal resistances between the nodes. Consequently, the heat is transferred quickly throughout the whole silicon chip.

Another difficulty in temperature modeling is the thermal behavior of the package and of the off-chip PCB interconnections and resonator. An analysis based on numerous measurements suggested that the thermal effects of the package and interconnections can be modeled by replacing the inductors in the package and interconnection models

Node	A	C	D	E	F
T_{chip}(°C)	55.5	56.7	55.4	55.4	56.1
T_{ref}(°C)	30.5	31.7	30.4	30.4	31.1

Table 1: Power dissipation in each block of the chip

with temperature sensitive ones, that is, inductances with temperature coefficients (TC's).

The bipolar transistors are modeled using Philips' Most EXquisite TRAnsistor Model (MEXTRAM), an advanced compact model [2] as implemented in HP's Microwave Design System (MDS) [3]. The temperature dependence of all the other on-chip and off-chip components were modeled as well. The validity of these models was assessed in practice.

3 Analysis

The oscillator to be analyzed and compensated is a wideband balanced oscillator, frequency tuned using a varicap, as shown in Figures 1 and 4. All properties of interest were

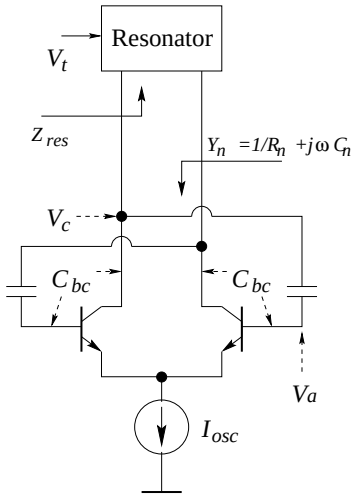

Figure 4: Oscillator circuit

analyzed both in terms of theory and experiment. The theoretical analysis based on temperature dependent models of all the components was carried out using HP's MDS. The harmonic balance simulator was employed for oscillation simulations. The output admittances Y_n (negative resistance R_n and capacitive load C_n) and resonant frequency of the off-chip resonator were simulated and measured under small signal conditions. The temperature dependence for all properties was analyzed at 0, 25, and 50°C.

Good temperature agreement has been obtained between simulations and measurements for DC biasing, output admittances, and resonant and oscillation frequencies. A comparison of measured and simulated deviations in resonant frequency and oscillation frequency as function of tuning voltage V_t at 0 and 50°C are displayed in Figures 5 and 6 with a reference temperature of 25°C. The frequency dependence on DC current, DC voltage and some on-chip resistances was investigated with particular care being paid to achieving wide-band compensation.

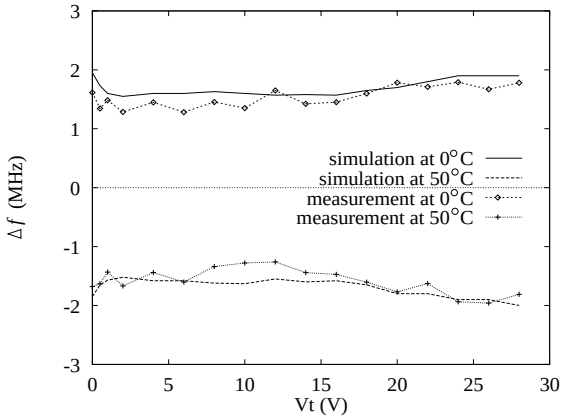

Figure 5: Simulated and measured frequency drift of resonant frequency with tuning voltage (reference temperature=25°C)

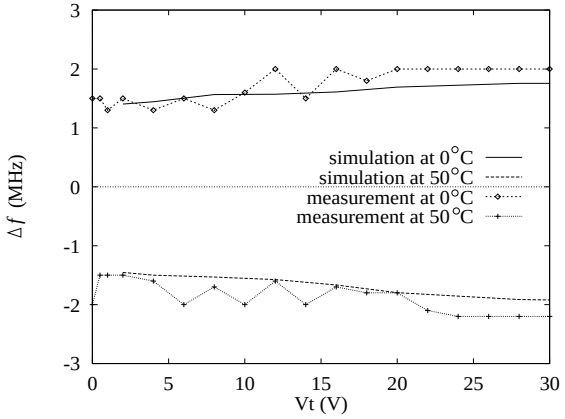

Figure 6: Simulated and measured frequency drift of oscillation frequency with tuning voltage (reference temperature=25°C)

4 Compensation Design

Temperature compensation design strategies were applied to achieve a goal of $\Delta f < \pm 500$ kHz at 0∼50°C, using DC voltage and resistance compensations. The oscillator schematic is given in Figure 4.

DC voltage compensation design is based on the frequency behavior as function of V_a and I_{osc}. This includes choosing best ranges for V_a, I_{osc} with appropriate temperature coefficients (TC). It was found that within the whole tuning range the dependence of the oscillation frequency on temperature is much greater at higher frequencies than at lower ones. Special techniques are necessary to prevent over-compensation at high frequencies and under-compensation at lower frequencies. Figure 7 illustrates one of these approaches: decreasing I_{osc} within the shadowed range results in positive frequency deviation at low frequencies (e.g. V_t=4 V) and negative frequency deviation at high frequencies (e.g. V_t=28 V).

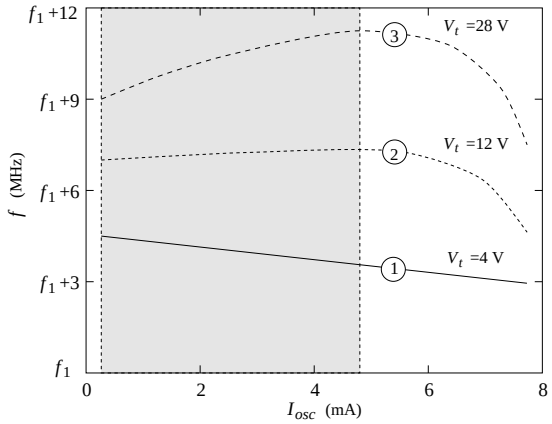

Figure 7: Frequency deviation with I_{osc} at various tuning voltages

Compensation using V_a is coupled to the voltage dependence of C_{bc} directly contributing to the output C_n. C_{bc} increases with temperature, and therefore lowers the oscillation frequency. Decreasing V_a and increasing V_c both can lower C_{bc} suggesting the use of a negative TC for V_a.

In summary, as presented in Figure 8, decreasing V_a suppresses the frequency deviation from curve 1 to curve 2. Reducing I_{osc} enhances this effect at low frequencies while simultaneously preventing over-compensation at high frequencies (see curve 3). Further compensation based on the choice of resistor-type moves curve 3 lower to curve 4. Two DC voltage sources decreasing with temperature have been designed to realize V_a and I_{osc} with negative TC's.

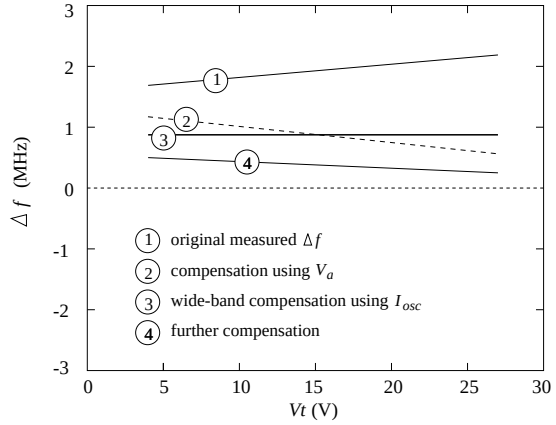

Figure 8: Wide-band compensation using DC method

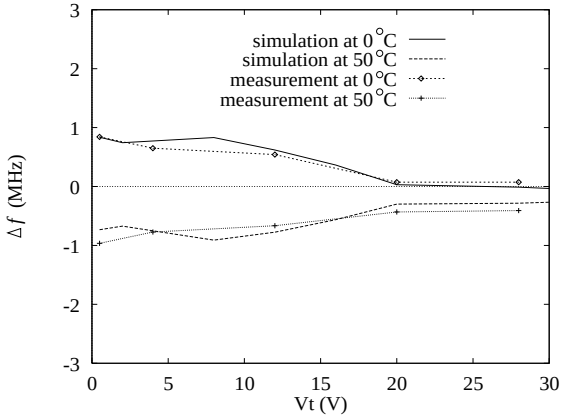

Figure 9: Comparison of simulated and measured frequency drift $\Delta f \sim T$ for testchip $\#1$ with tuning voltage (reference temperature=25°C)

Two schematics using different TC's (TC_1=-3000 ppm/°C for $\#1$ and TC_2=-4700 ppm/°C for $\#2$) for V_a were designed and integrated. In addition, the applied compensation should maintain proper VCO operation and have minimal affect on other properties.

5 Results

The final design implemented in the high frequency BiCMOS Qubic-process proved to be very well compensated for temperature. The overall frequency drift ($\Delta f \sim T$) has been theoretically reduced to less than $\pm$0.6 MHz and $\pm$1.0 MHz for designs $\#1$ and $\#2$, respectively, within the frequency range of interest (470 $\sim$930 MHz for V_t=0.5$\sim$28V) and satisfying the specified temperature range (0$\sim$50$^\circ C$). At most operating frequencies the frequency drift with temperature for $\#2$ is less than $\pm$0.5 MHz. Two testchips were realized and evaluated by measurement. As can be seen in Figures 9 and 10, in both cases excellent agreement with simulated $f \sim T$ characteristics have been demonstrated although the measured $\Delta f \sim T$ of $\#2$ has a slightly higher value than was simulated for $V_t < 4$ V.

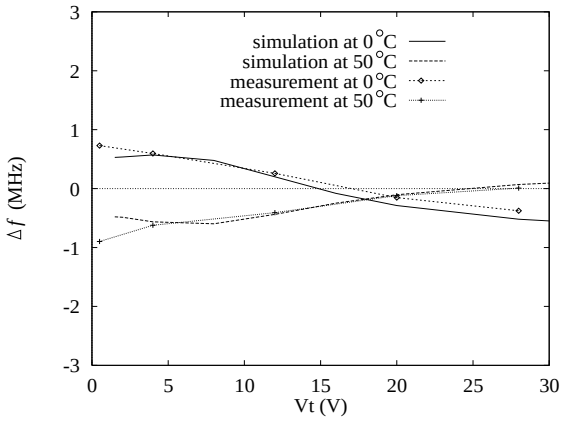

Figure 10: Comparison of simulated and measured frequency drift $\Delta f \sim T$ for testchip $\#2$ with tuning voltage (reference temperature=25°C)

6 Conclusions

This paper systematically describes the temperature modeling, analysis and the on-chip temperature compensation design of an UHF VCO integrated in the Qubic-process. Based on precise temperature modeling, the analysis and on-chip compensation have given accurate results. Excellent on-chip temperature compensation has been achieved. A VCO frequency-drift Δf <0.5 MHz is realized.

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